

REMARKS

At the outset, the Examiner is thanked for the thorough consideration given the subject application. Claims 1-19 are currently pending in this application. Claims 1, 6, and 10 have been amended. Reconsideration and reexamination are respectfully requested.

The Examiner objected to the claims because of informalities. Claims 1, 6, and 10 have been amended to correct the informalities. Applicants request that the objection be withdrawn.

The Examiner rejected claims 1, 3-7, and 9 under 35 USC 103(a) as being unpatentable over den Boer et al. (US Pat. No. 5,641,974) in view of Yoshino (US Pat. No. 5,358,810). Applicants respectfully traverse this rejection.

Claim 1 is allowable at least for the reason that claim 1 recites a combination of elements including a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line; a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and liquid crystals injected and sealed between the thin film transistor plate and the color filter plate, wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate.

Claim 6 is allowable at least for the reason that claim 6 recites a combination of elements including a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode; a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and liquid crystals injected and sealed between the thin film transistor plate and the color filter plate, wherein the pixel electrode

asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end.

None of the cited references, singly or in combination, teaches or suggests, at least these features of the claims.

In column 5, lines 20-31, den Boer et al. states: "Source electrode 15 is connected to pixel electrode 3 by way of via or contact hole 35 so as to permit TFT 9 to act as a switching elements and selectively energize a corresponding pixel in AMLCD 2 in order to provide image data to a viewer." In column 6, lines 62-64, den Boer et al. states: "Pixel electrodes 3 overlap address lines 5 and 7 along the edges thereof as shown in FIG. 1 by an amount of up to 3 μm ." In column 10, lines 37-65, den Boer et al. states: "Black matrix structure 55 includes vertically extending regions 56 and horizontally extending regions 57. Regions 56 are aligned with drain lines 5 while regions 57 are aligned with gate lines 7 so as to prevent ambient light from penetrating the display. Additionally, black matrix 55 includes channel covering portions 58 which are aligned with TFT channels 27 for the purpose of preventing ambient light from reaching amorphous silicon semiconductor layer 23 through the channels. As commonly known in the art, the pixel openings 65 of the display are substantially defined by (i.e. bounded by) black matrix regions 56 and 57." "Also, black matrix portions 56 line up with address lines 5 so that the pixel aperture or opening for the center electrode 3 is defined in part by the distance between black matrix members 56. Black matrix portions 56 and address lines 5 are both arranged so that their central axes correspond with the gaps between pixel electrodes 3 according to certain embodiments of this invention."

In contradistinction, in claim 1, the present application includes, a pixel electrode...being connected to the drain electrode through the contact hole, a color filter plate...on a second transparent substrate, wherein the black matrix of the color filter plate

asymmetrically overlaps the data line of the thin film transistor plate. In contradistinction, in claim 6, the present application includes, a pixel electrode...being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode, a color filter plate, and wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end.

The Examiner cites Yoshino in an attempt to cure the deficiencies of den Boer et al. However, even if Yoshino teaches a color filter plate, the references does not teach a color filter plate, wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate as in claim 1 or wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end as in claim 6. Yoshino fails to cure the deficiencies of den Boer et al.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness. Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

Moreover, claims 3-5, 7, and 9 are allowable by virtue of their dependence on claims 1 and 6, which are believed to be allowable.

The Examiner rejected claim 2 under 35 USC 103(a) as being unpatentable over den Boer et al. (US Pat. No. 5,641,974) in view of Yoshino (US Pat. No. 5,358,810) as applied to claims 1, 3-7, and 9 above, and further in view of Kobayashi et al. (US Pat. No. 5,847,792). Applicants respectfully traverse this rejection.

The Examiner cites Kobayashi et al. in an attempt to cure the deficiencies of den Boer et al. and Yoshino. However, even if Kobayashi et al. teaches the location of the black matrix, the reference does not teach a color filter plate, wherein the black matrix of the color filter plate

asymmetrically overlaps the data line of the thin film transistor plate as in claim 1 or wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end as in claim 6. Kobayashi et al. fails to cure the deficiencies of den Boer et al. and Yoshino.

Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

The Examiner rejected claim 8 under 35 USC 103(a) as being unpatentable over den Boer et al. (US Pat. No. 5,641,974) in view of Yoshino (US Pat. No. 5,358,810) as applied to claims 1, 3-7, and 9 above, and further in view of Hanazawa et al. (US Pat. No. 5,953,088). Applicants respectfully traverse this rejection.

The Examiner cites Hanazawa et al. in an attempt to cure the deficiencies of den Boer et al. and Yoshino. However, even if Hanazawa et al. teaches the overlapped width, the reference does not teach a color filter plate, wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate as in claim 1 or wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end as in claim 6. Hanazawa et al. fails to cure the deficiencies of den Boer et al. and Yoshino.

Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

The Examiner rejected claims 10-12, and 14 under 35 USC 103(a) as being unpatentable over Hanazawa et al. (US Pat. No. 5,953,088) in view of Murade (US Pat. No. 6,388,721). Applicants respectfully traverse this rejection.

Claim 10 is allowable at least for the reason that claim 10 recites a combination of elements including a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line; a color filter plate including a black matrix, a color filter and a common electrode on a

second transparent substrate; and liquid crystals injected and sealed between the thin film transistor plate and the color filter plate, wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode. None of the cited references, singly or in combination, teaches or suggests, at least these features of the claims.

In column 5, lines 46 to column 6, line 7, Hanazawa et al. '088 states: "Thereafter, signal lines 50a and 50b, a drain electrode connected between the signal line 50a and the drain region 66 of the pixel-use thin film transistor TR, a source electrode connected to the source region 67 and serving as an upper electrode 78 of the storage capacitance element, and wiring layers for the driver-use thin film transistors 71 and 68 are formed." "Thereafter, an organic insulation film 81 of a thickness of 2 μm to 4 μm is formed to cover the overall surface of the protection film 79, and a contact hole 82 is formed in the film 81 to expose the upper electrode 78 of the storage capacitance element. Finally, a transparent conductive material such as ITO is deposited by the sputtering to a thickness of about 100 nm and patterned to a predetermined shape by the photo-etching, thereby forming a pixel electrode 51 (PE) which contacts the upper electrode 78 of the storage capacitance element. The array substrate 83 is completed by the processes described above." In column 6, lines 8-15, Hanazawa et al. '088 states: "In the manufacturing step of the counter substrate 87, a colored layer 85, in which a pigment or the like is dispersed, is formed on a light-transmitting insulation plate 84, such as a glass plate. Further, a transparent conductive material such as ITO is deposited by sputtering to form a counter electrode 86 on the colored layer 85. The counter substrate 87 is completed through the processes described above." In column 7, lines 28-39, Hanazawa et al. states: "The array substrate 83 further comprises a plurality of storage capacitance lines 52 each formed across the pixel electrodes PE of a corresponding row in parallel with the scanning lines Y and set at a

predetermined potential, and a plurality of shield electrodes SH extending from the storage capacitance lines 52 and each capacitively coupled to a corresponding signal line X and two pixel electrodes PE adjacent to the corresponding signal line X. Each shield electrode SH is formed along the corresponding signal line X and arranged to alternately overlap one and the other of the two adjacent pixel electrodes PE.”

In contradistinction, in claim 10, the present application includes, a pixel electrode...being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line; a color filter plate, wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode.

The Examiner cites Murade in an attempt to cure the deficiencies of Hanazawa et al. ‘088. However, even if Murade teaches a black matrix, the reference does not teach a pixel electrode...being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line; a color filter plate, wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode as in claim 10. Murade fails to cure the deficiencies of Hanazawa et al.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness. Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

Moreover, claims 11, 12, and 14 are allowable by virtue of their dependence on claim 10, which is believed to be allowable.

The Examiner rejected claim 13 under 35 USC 103(a) as being unpatentable over Hanazawa et al. (US Pat. No. 5,953,088) in view of Murade (US Pat. No. 6,388,721), and further

in view of Hanazawa et al. (US Pat. No. 6,400,427) and den Boer et al. (US Pat. No. 5,641,974). Applicants respectfully traverse this rejection.

The Examiner cites Hanazawa et al. '427 and den Boer et al. in an attempt to cure the deficiencies of Hanazawa et al. '088 and Murade. However, even if Hanazawa et al. '427 and den Boer et al. teach the overlapped region, the reference does not teach a pixel electrode...being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line; a color filter plate, wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode as in claim 10. Hanazawa et al. '427 and den Boer et al. fail to cure the deficiencies of Hanazawa et al. '088 and Murade.

Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

The Examiner rejected claims 15-17, and 19 under 35 USC § 102(e) as being anticipated by Hanazawa et al. (US Pat. No. 5,953,088). Applicants respectfully traverse this rejection.

Claim 15 is allowable at least for the reason that claim 15 recites a combination of elements including simultaneously forming a gate line in the gate region wherein a gate electrode protrudes from the gate line, and a cut-off film which is asymmetrically overlapped by the data line region; forming a passivation layer covering the gate line region, the data line region and the cut-off film, wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer; and forming a pixel electrode connected to the drain electrode through the contact hole on the passivation layer, wherein the pixel electrode partially overlaps the cut-off film. None of the cited references teaches each and every feature of the claims.

Hanazawa et al. '088 has been discussed above. Further, no where in the reference states a method including simultaneously forming the gate line and the cut-off film. Additionally, contact hole 82 exposing a portion of the source electrode is formed in the passivation layer 81. The pixel electrode 51 is formed to connect to the source electrode.

Applicants respectfully submit that claim 15 is not anticipated because each and every feature as set forth in the claim cannot be found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully request that the rejection under 35 USC § 102(e) be withdrawn.

Moreover, claims 16, 17, and 19 are allowable by virtue of their dependence on claim 15, which is believed to be allowable.

The Examiner rejected claim 18 under 35 USC 103(a) as being unpatentable over Hanazawa et al. (US Pat. No. 5,953,088) in view of Hanazawa et al. (US Pat. No. 6,400,427) and den Boer et al. (US Pat. No. 5,641,974). Applicants respectfully traverse this rejection.

The Examiner cites Hanazawa et al. '427 and den Boer et al. in an attempt to cure the deficiencies of Hanazawa et al. '088. However, even if Hanazawa et al. '427 and den Boer et al. teach an overlap region, the references do not teach simultaneously forming a gate line..., and a cut-off film which is asymmetrically overlapped by the data line region; forming a passivation layer covering the gate line region, the data line region and the cut-off film, wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer; and forming a pixel electrode connected to the drain electrode through the contact hole on the passivation layer, wherein the pixel electrode partially overlaps the cut-off film as in claim 15. Hanazawa et al. '427 and den Boer et al. fail to cure the deficiencies of Hanazawa '088.

Applicants respectfully request that the rejection under 35 USC § 103(a) be withdrawn.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to

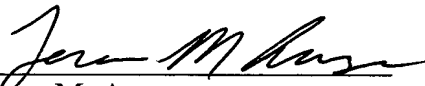
issue.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7371.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Dated: December 9, 2002

Respectfully submitted,

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Version With Markings to Show Changes Made

In the Claims

Please amend the claims as follows:

1. (Amended) A liquid crystal display comprising:

a thin film transistor plate further comprising:

a gate line on a first transparent substrate,

a data line arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor having a source electrode connected to the data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals injected and sealed between the thin film transistor plate and the color filter plate,

wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate.

6. (Amended) A liquid crystal display comprising:

- a thin film transistor plate further comprising:
 - a gate line on a first transparent substrate,
 - a first data line arranged to cross the gate line wherein the gate line is insulated from the data line,
 - a gate electrode protruding from said gate line in an area where said data line crosses said gate line,
 - a thin film transistor having a source electrode connected to the first data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other,
 - a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer, and
 - a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode;
 - a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and
 - liquid crystals injected and sealed between the thin film transistor plate and the color filter plate,
- wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end.

10. (Amended) A liquid crystal display comprising:

- a thin film transistor plate further comprising:

a gate line on a first transparent substrate,

a data line arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor having a source electrode connected to the data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other;

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer; and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals injected and sealed between the thin film transistor plate and the color filter plate,

wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode.